REMARKS/ARGUMENTS

Status of Application

Claims 1-4 are pending in the subject application. Claims 1-4 are rejected under 35 USC § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter. Claims 1-2 are also rejected under 35 USC § 102 (b) as being anticipated by US Patent 5,148,435 (Ray et al.). Claims 3 and 4 are rejected under 35 USC § 103 (a) as being unpatentable over Ray et al. in view of US Patent No. 5, 330, 931 (Aunio et al.) and US Patent No. 5,742,589 (Murata et al.) respectively. Additionally, the drawings are objected to. By way of this response, Applicants have cancelled claims 1-4 without prejudice and added new claims 5-15.

Objections to the Drawings

The drawings are objected to by the Examiner for failing to include the first and second circuit node recited in claim 1. Applicants have cancelled claim 1, rendering this basis of objection moot. The drawings are further objected under 37 CFR 1.84(p)(5) for failing to include reference sign 6 referred to in the specification. In response, Applicants have amended Figures 1a and 2a to include the reference sign 6. Amended Figures are included in the attached Replacement Sheets for Examiner's approval.

Rejections under 35 USC § 112

Claims 1-4 stand rejected under 35 USC § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Applicants have cancelled claims 1-4 without prejudice, thus rendering this basis of rejection moot.

Rejections under 35 USC § 102

Claims 1-2 stand rejected under 35 USC § 102 (b) as being anticipated by US Patent 5,148,435 (Ray et al.). Applicants have cancelled claims 1-2 without prejudice, thereby rendering the rejection moot.

Applicants, by way of this response, have added new claims 5-15 which more clearly recite the invention. The claims recite a method for verifying the functionality of a circuit

comprising a plurality of circuit blocks at the design level. Verification of functionality at the design level (e.g., VHDL level) allows for significant reduction of development costs as errors can be detected at the early stages of circuit development. Testing of circuit functionality at the design level is described in the specification. See Specification at page 3, lines 16-19 and page 8, lines 6-15. Applicants therefore submit that new claims do not include any new matter.

In contrast to the new claims, Ray et al. only describes circuit arrangements for data communications devices that enable testing by DTE/network management controller to identify when a fault has developed in the equipment. Detection of faults is performed on operational equipment, not at the design level. Verification of circuit functionality at the design level is nowhere taught or suggested by Ray et al. Therefore, Applicants submit that the newly added claims are patentable over Ray et al.

Rejections under 35 USC § 103

Claims 3-4 stand rejected under 35 USC § 103 (a) as being unpatentable over Ray et al. in view of US Patent No. 5,330,931 (Aunio et al.) and US Patent No. 5,742,589 (Murata) respectively. Claims 3-4 have been cancelled without prejudice by way of this response, rendering this basis of rejection moot.

With respect to newly added claims 5-15, these claims recite a method for verifying circuit functionality of a design level circuit having a plurality of circuit blocks. Ray et al., as already discussed above, only describes circuit arrangements that enable testing by DTE/network management controller to identify when a fault has developed in the equipment. Aunio et al. describes a method and arrangement for improving data transmission of an RF transceiver, while Murata describes a radio apparatus that uses its own receiver/transmitter to perform loopback tests for checking functionality of the apparatus during an unassigned receiving/transmission slot. None of the cited references, alone or in combination, teaches or suggests verifying a design level circuit having a plurality of circuit blocks. Therefore, Applicants submit that the newly added claims are patentable over the cited art, alone or in combination.

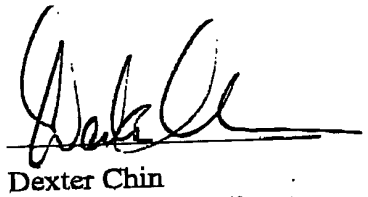
Conclusion

In view of the foregoing, Applicants believe that all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Dated: June 19, 2003

Respectfully submitted,



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Response dated June 19, 2003
Response to Office Action of December 19, 2002

Replacement Sheet

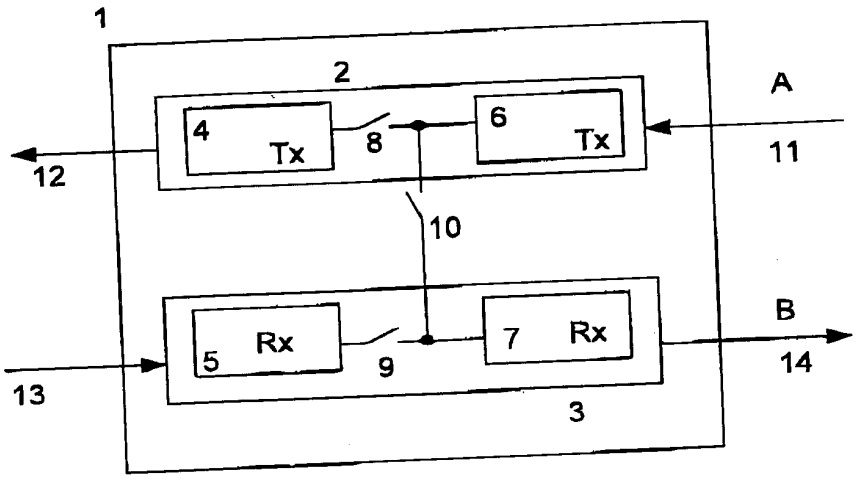

Fig. 1a

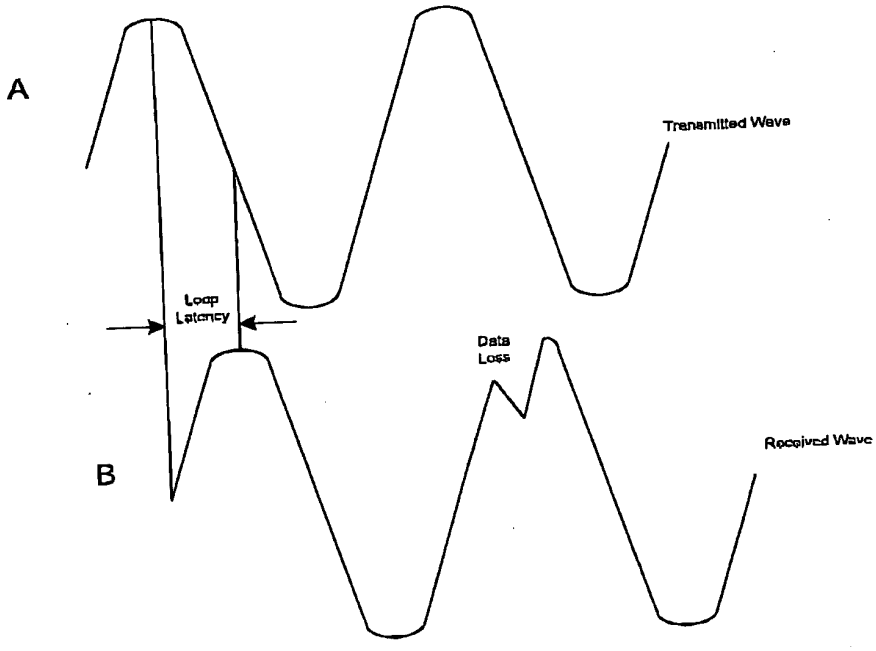

Fig. 1b

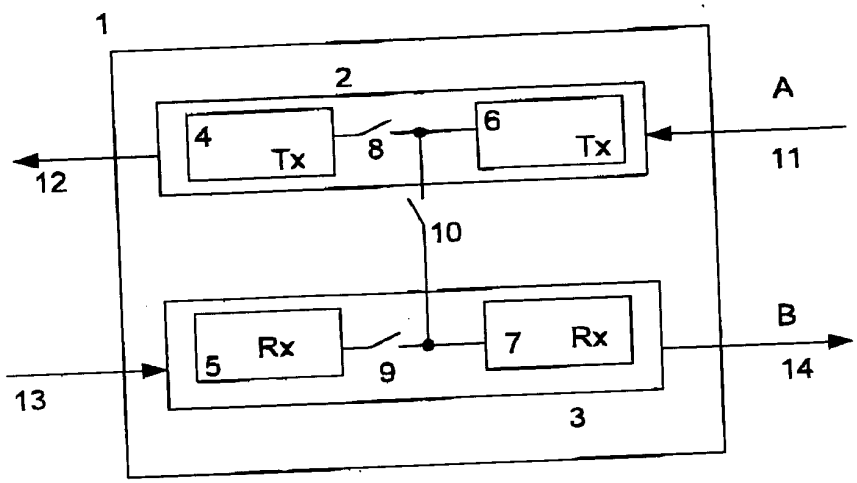
1
2
A
4
Tx
8
6
Tx
12
11
10
B
5
Rx
9
7
Rx
14
13
3

Fig. 2a

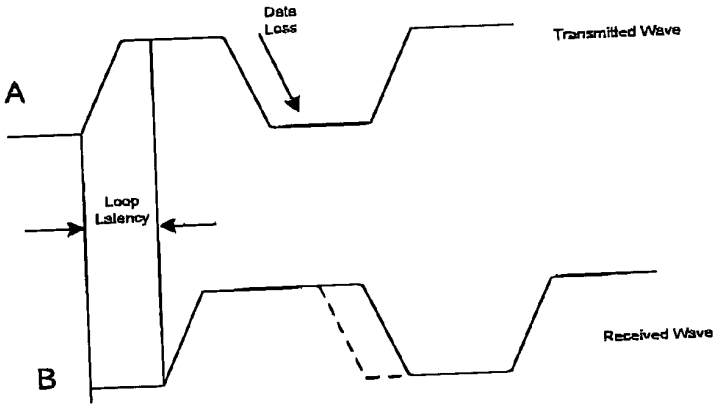
Data
Loss
Transmitted Wave
A
Loop
Latency
Received Wave
B

Fig. 2b